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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/526,864	03/04/2005	Alan G. Knapp	GB 030093	5468

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EXAMINER	
WALTHALL, ALLISON N	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
12/17/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/526,864	KNAPP ET AL.	
	Examiner	Art Unit	
	ALLISON WALTHALL	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 18-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 18-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed September 17, 2009 has been entered.

Claim Objections

2. Claims 2-9, 19-21 and 23-24 are objected to because "overall brightness" should be changed to "combined brightness".

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 4, 18, 19, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura (6,518,962) in view of Onagawa (US Patent 7,042,524).

As to **claims 1 and 18**, Kimura discloses an active matrix electroluminescent display device including an array of display (FIG. 1) comprising: an electroluminescent display element (224);

active matrix circuitry including at least one drive transistor (223) for driving a current through the display element (col. 20 lines 50-57);

means for determining a brightness level (current measuring equipment 16 + comparison circuit 21a, col. 21 lines 57-59) of a pixel; and means for controlling

(Voltage control circuit 22c, see FIG. 6, column 23, lines 39-46 and column 23 line 61-column 24 line 14) the at least one drive transistor (223) of each pixel in dependence on a respective input signal (Vsig) providing a drive level for the pixel and in dependence on the brightness level (current ID).

Kimura does not disclose means for determining a combined brightness level of a multitude of pixels in an image to be displayed in a frame period; and means for controlling the at least one drive transistor of each pixel individually in dependence on a respective input signal providing a drive level for the pixel and in dependence on the combined brightness level of the multitude of pixels in the image.

Onagawa teaches means for determining a combined brightness level of a multitude of pixels in an image to be displayed in a frame period (see figure 2 and column 5, lines 1-5); and means for controlling each pixel individually in dependence on a respective input signal providing a drive level for the pixel and in dependence on the combined brightness level of the multitude of pixels in the image (see figure 4A and figure 5). It would have been obvious to one having ordinary skill in the art at the time the invention was made to determine a combined brightness level of a multitude of pixels, as taught by Onagawa instead of the brightness level of a single pixel, in order to reduce flicker.

As to **claims 2 and 19**, Kimura discloses wherein the means for controlling the at least one drive transistor comprises a signal processing device (current measuring equipment 16 + comparison circuit 21a + voltage control circuit 22c + controller 23) for determining the brightness level (measured current indicates the overall brightness

level) and for processing the input signals for the pixels in dependence on the brightness level (measured ID is compared to a reference and the voltage control circuit adjusts accordingly). Onagawa teaches a signal processing device (figure 1) for determining the combined brightness level and for processing the input signals (video data in) for the pixels in dependence on the combined brightness level (see 7, 3, 11-13 producing video data out). Therefore the combination of the Kimura and Onagawa meets the claim limitations for the reason cited above.

As to **claims 4 and 22**, Kimura discloses wherein the signal processing device is adapted to employ gamma characteristics for processing the input signals in dependence on the brightness level (Kimura discloses the use of well-known processing circuit 1002 using a gamma- correction circuit, col. 40 lines 17-21).

5. Claims 3, 5-7, 20 and 23 rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura in view of Onagawa as applied to claims 1 and 18 above, and further in view of Mori (US Publication 2003/0025718).

As to **claims 3 and 20**, Onagawa teaches a summation unit for summing the input signals for the multitude of pixels of the image to determine the combined brightness (see figure 2) but Onagawa does not specifically teach the signal processing device comprises a field store for storing the input signals for an image, and a summation unit for summing the input signals for the multitude of pixels of the image in the field store to determine the overall brightness.

However, Mori discloses a signal processing device comprises a field store (frame memory 4) for storing the input signals for an image (see [0036]); and a summation unit (Brightness Detection Unit which detects using an integrator to determine the brightness information of the input video signal, paragraph [0038]) for summing the input signals for the multitude of pixels of the image in a field store (Frame memory 4) to determine the combined brightness. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the field store of Mori in the signal processing device of Kimura as modified by Onagawa, in order to conduct digital ABL processing (see [0134]).

As to **claim 5 and 23**, Mori discloses wherein the signal processing device further comprises a look up table (Table used to conduct calculations, Page 7 paragraphs [0113]-[0114]) for modifying the input signals for the stored image in dependence on the overall brightness level.

As to **claim 6**, Mori discloses wherein the signal processing device is adapted to calculate the look-up table in dependence on the overall brightness level (Page 7 paragraphs [0113]-[0114]).

As to **claim 7**, Mori discloses wherein the signal processing device operates to reduce the maximum brightness level to which any pixel is drive in response to an increase in the overall brightness of an image (The display panel brightness level is reduced if the mean brightness is high, Page 3 paragraph [0044]).

6. Claims 8, 21, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura in view of Oganawa, as applied above to claim 2, and further in view of Feldman (US Patent 6,582,980).

As to **claims 8 and 24**, Kimura in view of Oganawa discloses a device as claimed in claim 2, but does not specifically disclose wherein the signal processing device comprises digital to analogue converter circuitry for converting digital inputs into the input signal, and wherein the digital to analogue converter circuitry is controllable in dependence on the overall brightness level.

However, Feldman discloses a signal processing device (Signal processing circuit 14) comprises digital to analogue converter (Display Driver 30 may contain a digital-to-analog converter, col. 11 lines 60-67) circuitry for converting digital inputs into the input signal, and wherein the digital to analogue converter circuitry is controllable in dependence on the overall brightness level (The signal processing circuit processes the overall brightness level and supplies the signal to the display driver, wherein the digital to analog converter converts the signal.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have modified the signal processing circuit as taught by Feldman to have an digital to analog converter within the signal processing circuit of Kimura as modified by Onagawa for the purpose of producing analog signals for image display that expect analog drive (col. 11 lines 63-65).

As to **claim 21**, Feldman discloses wherein processing the input signal comprising modifying the input signals using a look up table (Table lookup logic, col. 10

lines 4-9), the address of which is selected in dependence on the input signal and the overall brightness level.

7. Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura in view of Onagawa, as applied to claim 1 above, and further in view of Feldman and Murai et al. (JP application JP 2001-1305511 A).

As to **claim 9**, Kimura in view of Onagawa discloses a device as claimed in claim 1, but does not specifically discloses wherein the active matrix circuitry comprises first and second drive transistors in parallel each connected between a respective power supply line and the EL display element, the input to the pixel being provided to the gates of the first and second drive transistors, and wherein the first the drive transistor is supplied with a first supply voltage and the second drive transistor is supplied with a second supply voltage, at least one of the supply voltages being variable in dependence on the on the overall brightness level.

However Murai discloses in FIG. 6 wherein a active matrix circuitry comprises first and second drive transistors (Transistors 14 and 13, respectively) in parallel each connected between a respective power supply line (Lines 1012 and 3, respectively) and the display element (Element 1102), the input to the pixel being provided to the gates of the first and second drive transistors (14 and 13, respectively), and wherein the first the drive transistor (14) is supplied with a first supply voltage (Voltage seen in FIG. 4e) and the second drive transistor (13) is supplied with a second supply voltage (Voltage seen

in FIG. 4c), at least one of the supply voltages being variable in dependence on the on the overall brightness level (Page 11 and bottom half of paragraph [0030]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have modified the active matrix circuitry as taught by Murai in place of the circuitry of Kimura as modified by Onagawa to use two drive transistors for the purpose of lower power dissipation (Page 11 and bottom half of paragraph [0030]).

Although Murai uses a Liquid crystal element, the Feldman reference teaches LCD panels and other flat-panel display, such as Electroluminescent display, technologies employ similar device structures (col. 1 lines 29-34).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have used the circuitry structure as taught by Murai in place of Display structure of Kimura as Feldman teaches to employ the benefit of lower power dissipation in a display panel as suggested above by Murai.

As to **claim 10**, Murai discloses in FIG. 6 wherein the input to the pixel is provided to the gates of the first and second drive transistors (14 and 13, respectively) through an address transistor (Transistor 11).

As to **claim 11**, Murai discloses wherein the first supply voltage (FIG. 4e) is fixed and the second supply voltage (FIG. 4c) is variable (The interval of Power Line 3 can be varied, Page 11 and bottom half of [0030]).

As to **claim 12,** Murai discloses wherein the first and second supply voltages can be equal (Lines 1012 and 3, respectively, are the same electric potential, Page 11 paragraph [0029]).

Response to Arguments

8. Applicant's arguments with respect to claims 1 and 18 have been considered but are moot in view of the new ground(s) of rejection. In view of amendments, the reference of Onagawa has been added for new grounds of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALLISON WALTHALL whose telephone number is (571)270-3571. The examiner can normally be reached on Mon - Fri 9:30-6:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

anw
December 8, 2009

/Chanh Nguyen/
Supervisory Patent Examiner, Art Unit 2629